WHAT IS CLAIMED IS:

1. A method comprising:

patterning a substrate with a substantially arbitrary arrangement of features by introducing irregularity into an array of repeating lines and spaces between the lines.

2. The method of claim 1, wherein introducing irregularity comprises forming an arbitrary figure above the array.

3. The method of claim 2, wherein patterning the substrate further comprises etching a substrate through portions of the array not covered by the arbitrary figure.

4. The method of claim 1, wherein introducing irregularity comprises reducing the continuity of at least a portion of the array, the array formed using an interference lithography system.

5. The method of claim 4, wherein reducing the continuity of the portion of the array comprises cutting spaces in the array.

6. The method of claim 1, wherein introducing irregularity comprises reducing the continuity of the portion of the array resulting from a projection lithography patterning.

7. The method of claim 1, wherein patterning the substrate further comprises etching the substrate using the substantially arbitrary arrangement to direct the etching.

8. The method of claim 1, wherein patterning the substrate further comprises patterning the substrate with the substantially arbitrary arrangement having a pitch yielding a k_1 factor smaller than or equal to 0.4.

9. A device, comprising:

a substantially arbitrary arrangement of trenches, the trenches defined with a definition characteristic of interference lithography.

10. The device of claim 9, wherein the substantially arbitrary arrangement of trenches comprises trenches including discontinuities at varying positions along the trenches.

11. The device of claim 9, wherein the substantially arbitrary arrangement of trenches comprises features printed with a pitch yielding a k_1 factor smaller than or equal to 0.5.

12. The device of claim 11, wherein the substantially arbitrary arrangement of trenches comprises trenches with

a pitch yielding a k_1 factor approaching 0.25 for a single patterning step.

13. The device of claim 9, wherein the substantially arbitrary arrangement of trenches comprises trenches free from defects arising due to one or more of lens imperfections and mask imperfections.

14. The device of claim 9, wherein the substantially arbitrary arrangement of trenches comprises trenches free from defects arising due to backscatter of electrons.

15. The device of claim 9, wherein the substantially arbitrary arrangement of trenches comprises a portion of a microelectronic device.

16. A method comprising:

interfering electromagnetic radiation to illuminate a substrate with an interference pattern, the interference pattern imparting the substrate with repeating lines and spaces; and

introducing irregularity into the interference pattern to impart an arbitrary feature arrangement to the substrate.

17. The method of claim 16, wherein introducing irregularity comprises ending continuity of a trench at an arbitrary position along the trench.

18. The method of claim 16, wherein introducing irregularity comprises forming an arbitrary figure above some portion of the repeating lines and spaces.

19. The method of claim 16, wherein introducing irregularity comprises forming an arbitrary figure in some portion of the repeating lines and spaces.

20. The method of claim 17, further comprises patterning the substrate using the arbitrary figure to define the arbitrary feature arrangement.

21. The method of claim 16, wherein interfering electromagnetic radiation comprises imparting, to the substrate, first features having a pitch yielding a k_1 factor approaching 0.25 in a single patterning step.

22. A method comprising:

patterning a substrate using a first lithographic technique, the patterning providing lines and spaces with a first pitch yielding a first k_1 factor smaller than or equal to 0.5; and

eliminating the impact of at least some of one or

more portions of the lines and spaces on the substrate using a second lithographic technique providing second features with a second pitch, the second pitch two or more times larger that the first pitch.

23. The method of claim 22, wherein patterning the substrate using the first lithographic technique comprises providing first lines and spaces with the first pitch yielding the first k_1 factor approaching 0.25 for a single patterning step.

24. The method of claim 22, wherein patterning the substrate using the first lithographic technique comprises patterning the substrate using interference lithography.

25. The method of claim 22, wherein eliminating the impact comprises patterning using a binary mask.

26. The method of claim 22, wherein eliminating the impact comprises using the second lithographic technique providing second features with the second pitch yielding the second k_1 factor greater than 0.5.

27. The method of claim 22, wherein eliminating the impact comprises printing an arbitrary figure above some of the spaces.

28. The method of claim 27, wherein eliminating the impact comprises etching a portion of the substrate not covered by the arbitrary figure.

29. The method of claim 27, wherein eliminating the impact comprises ending continuity of at least one or more portions of the lines and spaces.

30. An apparatus comprising:

an interference exposure module to produce a first exposure resulting in an array of repeating features in a photosensitive media; and

a second patterning module to reduce regularity of the features in the array.

31. The apparatus of claim 30, further comprising an alignment sensor to align a second exposure pattern produced by the second patterning module with the array.

32. The apparatus of claim 30, further comprising a common control system to regulate the interference exposure module and the second patterning module.

33. The apparatus of claim 30, further comprising a common wafer stage to present a wafer to the interference exposure module and to the second patterning module.

34. The apparatus of claim 30, wherein:

the interference exposure module comprises an interference lithography module; and

the second patterning module comprises a projection optical lithography system, the projection optical lithography system including

a mask to reduce regularity in the array created by the interference exposure module,

projection optics, and

a wafer stage.

35. A method comprising:

receiving a design layout of a layout piece;

receiving an interference pattern array layout;

determining a difference between the design layout and the interference pattern array layout; and

generating a print mask using the determined difference.

36. The method of claim 28, wherein generating the print mask comprises resizing a remainder array reflecting the difference between the design layout and the interference pattern array layout.